REMARKS

Reconsideration of the objection and the rejections set forth in the Office Action dated June 27, 2005, is respectfully requested. The Examiner rejected claims 5, 7, and 9 and objected to claims 6 and 8. Applicants have canceled claims 5-9 and have added new claims 10-20. Accordingly, claims 10-20 remain pending in the application. No new matter has been added by these amendments as can be confirmed by the Examiner.

A. Submission of Formal Drawings.

In the Office Action, the Examiner objected to the drawings filed on September 6, 2005, and required new corrected drawings in compliance with 37 C.F.R. § 1.121(f). Applicants therefore submit herewith a set of formal drawings for the present application. Current USPTO drafting requirements necessitated that Fig. 1 be disposed on four separate drawing sheets. The figures on the four drawing sheets have been respectively designated as Figs. 1B-E; whereas, Fig. 1A illustrates the arrangement of Figs. 1B-E to form the original Fig. 1. Applicants further submit herewith appropriate amendments to the specification to reflect the division of Fig. 1 into Figs. 1A-E. No new matter has been added.

B. Allowable Subject Matter.

The Examiner rejected claims 5, 7, and 9 under 35 U.S.C. § 102(a) as allegedly being anticipated by Liu et al., United States Patent No. 6,026,230, and objected to claims 6 and 8. Applicants note with appreciation the Examiner's indication that claims 6 and 8 would be allowable if rewritten in independent form, including the limitations of the base claim and any intervening claims. Accordingly, Applicants submit new claims 10-20 that are based upon allowable claims 6 and 8. Therefore, it is submitted that claims 10-20 are in condition for allowance.

C. The Prior Art Does Not Disclose or Suggest the Use of Processors and Data Memory with Differing Operate Clock Rates in Accordance with Claims 10-20.

As recognized by the Examiner, none of the prior art, including Liu et al., discloses or renders obvious an emulation engine, "wherein said memory has an operating clock rate for read operations that is twice an operating clock rate of said processors." In accordance with the Examiner's statement, Applicants submit that none of the prior art, including Liu et al., discloses or renders obvious new independent claims 10, 13, and 17, each reciting, *inter alia*, "a data memory having ... an operating clock rate" and "an operating clock rate of said processors differing from said operating clock rate of said data memory." Applicants therefore submit that, by failing to disclose each and every element of new independent claims 10, 13, and 17, Liu et al. does not anticipate new claims 10, 13, and 17.

At least one recited element of claims 10, 13, and 17 therefore is totally missing from the prior art, including Liu et al. In accordance with M.P.E.P. § 2131, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). The disclosure of a claim element in a prior art reference, when relied upon to negate patentability, must also be clear and unambiguous. Further, "[t]he identical invention must be shown in as complete detail as contained in the...claim." *Richardson v. Suzuki Motor Corp.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Furthermore, and uniquely important in this case is the requirement that the elements relied on in the prior art reference must be arranged as required by the claim. See *In re Bonds*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990).

Accordingly, since the prior art, including Liu et al., fails to disclose each and every element of new independent claims 10, 13, and 17, the prior art does not

anticipate claims 10, 13, and 17, as well as new claims 11, 12, 14-16, and 18-20 that respectively depend thereon. Therefore, it is submitted that claims 10-20 are in condition for allowance.

D. No Motivation Exists to Modify the Teachings of the Prior Art in a Manner that Precludes the Patentability of New Claims 10-20 Under 35 U.S.C. § 103.

In accordance with M.P.E.P. § 2142, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met." (M.P.E.P. § 2143.) First, some suggestion or motivation in the prior art references or in the knowledge of one of ordinary skill in the relevant art must exist to modify or combine the references. Second, if the references are combined, a reasonable expectation of success must be shown. Then, finally, all of the claim limitations must be taught or suggested by one reference or a combination of references. To establish a *prima facie* case of obviousness based on a single reference that does not teach all the elements of a claim, the Examiner must provide a rationale for modifying the teachings of the reference. See *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000), *citing*, *B.F. Goodrich Co. v. Aircraft Breaking Sys. Corp.*, 72 F.3d 1577, 1582, 37 U.S.P.Q.2d 1314, 1318 (Fed. Cir. 1996).

In the manner discussed in more detail above, at least one recited element of claims 10, 13, and 17, therefore is totally missing from the prior art, including Liu et al. For example, as recognized by the Examiner, none of the prior art discloses or renders obvious an emulation engine, "wherein said memory has an operating clock rate for read operations that is twice an operating clock rate of said processors." Further, the Examiner does not assert that any teaching or motivation exists to modify the prior art in a manner that renders new claims 10-20 obvious. First, the Examiner has not established a *prima facie* case under 35 U.S.C. § 103 because, as shown above, all of the elements of the pending claims are not found in the cited reference. According, it is

submitted that the prior art, including Liu et al., does not render new claims 10-20 obvious. Applicants therefore assert that claims 10-20 are in condition for allowance.

For at least the reasons set forth above, it is submitted that new claims 10-20 are in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is encouraged to contact the undersigned at (949) 567-6700 if there is any way to expedite the prosecution of the present application.

Respectfully submitted,

Orrick, Herrington & Sutcliffe LLP

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By: Davin M. Stockwell

Davin M. Stockwell
Reg. No. 41,334
Attorneys for Applicants

Orrick, Herrington & Sutcliffe LLP
4 Park Plaza, Suite 1600
Irvine, California 92614-2558
Telephone: (949) 567-6700
Facsimile: (949) 567-6710

APPENDIX

Version with Markings to Show Changes Made to the Specification

Changes made to the paragraph starting on page 7, line 12:

[Figure 1 is] Figures 1A-E are a block diagram of a four processor cluster of the type more fully described in copending application serial no. 09/373,125, and included here to illustrate the technology state from which this invention departs.

Changes made to the paragraph starting on page 7, line 16:

Figure 2 is a block diagram of the cluster of [Figure 1] Figures 1A-E (shown in less detail than in [Figure 1] Figures 1A-E with multiplexed read port input and data memory in accordance with the teachings of this invention.

Changes made to the paragraph starting on page 7, line 21:

Referring now to [Figure 1] Figures 1A-E, as described more completely in application serial no. 09/373,125, each cluster of four processors (Processor0, Processor1, Processor2 and Processor3) has a shared data and input memory stack to which and from which each processor in the cluster can write and read. In this exemplary emulation processor, the memory stack has 256 addressable eight- bit words. Each processor has four read ports for reading an eight-bit word from the data memory comprised of address inputs RA0; RA1; RA2; and RA3 and corresponding inputs to the four eight-to-one multiplexers whose select inputs are TAC0; TAC1; TAC2 and TAC3 respectively. One each clock cycle, the inputs of the eight-to-one multiplexer of each of the four processors receives an eight-bit word from the memory. While generally satisfactory, there are a large number of processors (e.g. 64) and a correspondingly large number of memory stacks on a single ET 4 emulator chip. Silicon real estate is in short supply and the stack memory output ports take up a lot of area on the chip.